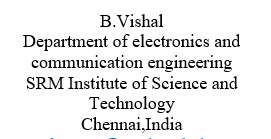
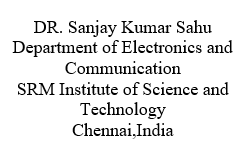
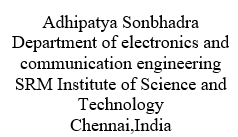
**Comparative analysis of multi-operand binary tree adder using different adder structures**

  
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***Abstract*— Binary tree adders (BTAs) are important components in hardware as they allow multiple operators to be added by combining two operand adders into a binary tree arrangement. The levels in binary tree in which there are adders performing concurrent computations, those levels scale as O(log2N), where N is the no. of operators . Therefore, the latency of the BTA is highly dependent on the number of operators and the latency of the aggregator. Various adder types, including traditional RCAs, carry-select adders, carry-advance adders, carry-skip adders, and BTAs using AOI-OAI-based RCAs, can be adjusted for link delays, slices, and LUT usages and powers Comparison for.**

**These architectures can be built in Verilog on Xilinx ISE and integrated into Spartan 3E.**

Keywords—Binary Tree adder,Verilog,Spartan3E

# Introduction

ULSI design technologies are the present focus of the electronics industry. Finding the best CPU design requires weighing architectures based on power consumption, latency, and area, which frequently compete with one another. Technology advancements have made power dissipation a major worry, and improving power is important for longer battery life. Additionally, for multitasking performance on contemporary CPUs, the region has become crucial to optimise. Adders are essential for attaining these goals in data route design because they help processing units respond more quickly, which is another important design requirement. The choice of adder is a significant design choice since arithmetic circuits consume a lot of resources. A compressor tree design may be used to represent multi-operand adders and is in charge of lowering the propagation carry and partial sum.

In many different applications, including floating-point units [1] and digital signal processing [2], multi-operand adders are essential components. Multi-operand adders are often used and easily implemented using binary tree adders (BTAs). The adders utilised inside the structure have a significant impact on the performance of a BTA in terms of delay and energy consumption[3]. There are several adders available to one in the field of BTA design. These include the skip and Carry-Select variations as well as RCA, CLA Adders. When choosing an adder[4] for a BTA structure to satisfy specific design criteria, designers must carefully evaluate these variables. Each type of adder has distinct advantages and trade-offs involving space, delay, and energy usage. Because of this, it is vital to assess the BTA utilising these various adder structures and choose the best design depending on particular needs.

When N is the no. of operands and T-adder is the adder's delay, the delay equation for a binary tree adder (BTA) is given as TBTA = log2N \* T-adder.

# Related Work

Since collectors are essential to bus design, considerable effort has been put towards improving them. In this work, numerous binary adder designs are identified, evaluated, and their outcomes in terms of field, latency, and power consumption are analysed. Computer-aided design approaches are used in research to synthesise and improve various collector topologies. The performance of various novel dual adder designs is contrasted with that of current adders in this article [5]. The gives a technique for preprogramming with little logic to optimise the space and latency of a transport adder.

Instead, it implements crossover logic using combinational gates like AOI and OR-AND-Invert [6]. On a Virtex 5 FPGA, Sudhir and Rajendra performed a research evaluating the power, latency, and LUTs of several collector topologies (such as RCA, CLA, and Koggestone collectors). [7].

We were able to examine the functionality of these adders in multi-person adders thanks to a comparative analysis of several 4-bit adders by Xilinx [4], including carry-select and carry-look-ahead-pavement adders.,.

# Adder used in BTA

1.Ripple Carry adder

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Surges from the whole adder block are carried by a surgecarry adder, as the name implies. As can be seen in Figure 1, the carry from the first adder is propagated to the next adder, which is the right course of action. finish the next adder The Nth full adder must wait for the N-1 full adders that came before it, which is the primary source of fluctuation, if the adder is suitable for the amount of adders. [5]

2.OAI-AOI based RCA

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By employing alternate AOI-OAI blocks, the AOI-OAI, also known as the surge transport adder , intends to decrease RCA latency and power usage, which will also decrease BTA-RCA latency and power. The surge transport collector is designed and modified using aoi-oai logic[6].

3.Carry lookahead adder

Graphical user interface, application

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Pre-transport adders use more complicated circuitry to reduce propagation latency. To limit the carry logic to small groups in the collector for the two logic levels, this design takes the role of the ripple transport design. A hand-maintained logic called Ci-1 = G0 + P0C0, where G stands for the producer and P0C0 for the promoter, provides the carry time in a hand-maintained adder .

4.Carry skip adder

Graphical user interface, application

Description automatically generated

The carry adder, often referred to as the carry bypass adder, lengthens the surge carry adder's delay. It has a multiplexer, n-input AND gate, and n-bit transport ripple chain. Despite using an unusual transport hopping adder in our design, Milid Bhadori's AOI-OAI logic is utilised [7].

5. Carry select adder

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It is possible to add two n-bit values using a carry-select adder. It has a multiplexer and two surge transport adders. This is done twice to do the addition: once while assuming the carry is zero and once again when assuming one. Two adders are used to do this.

after the addition is done twice, utilises a multiplexer to choose the right total and shift it to the right carry value .

IV.Proposed Methedology

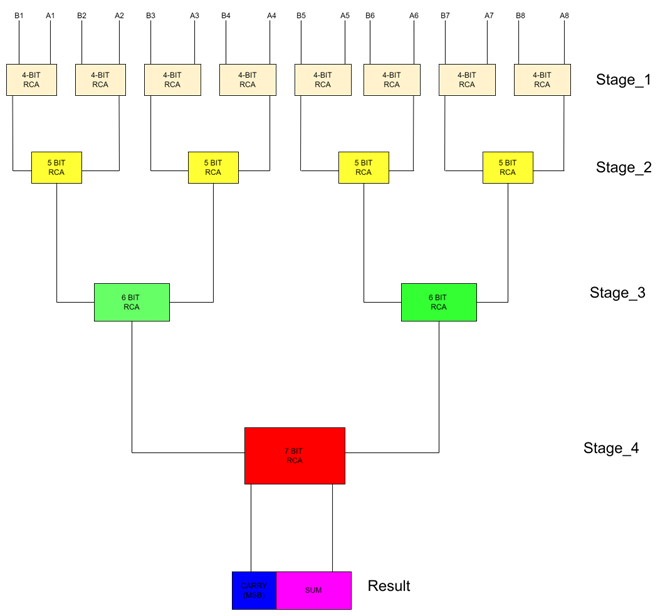
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Figure Methodology

The process carried out by us in designing and comparing different BTA architectures is shown. This process is repeated for all five architectures and after collecting data these architectures are compared and analyzed.

This laborious work will be helpful for digital designers in selecting optimal design for their desired application



Figure

We have created a common BTA architecture for 8 operand wherein we are changing the adders in each stage like in fig 2 it is shown for 16 operands of 4 bit instead we are designing and doing a comparative analysis of 8 operands BTA

The development of digital circuits requires the use of specific tools and techniques to ensure an optimal design. In this project, Xilinx ISE tool v14.7 was selected as the primary tool for designing and implementing digital circuits. All the modules in the project were written in Verilog HDL, including the testbench. The modules were then synthesized and implemented using Xilinx ISE to extract parameters such as combinational path delay and LUTs utilization. Simulation was performed using ModelSim.

To evaluate the performance of different architectures, power analysis was conducted using Xpower analyzer to extract dynamic power consumption for each design. A table was constructed to compare the different architectures in terms of parameters like combinational path delay, slice utilization, and dynamic power consumption. The data collected from the implemented designs were then used to plot graphs , which helped in visualizing and comparing the different architectures.

Finally, based on the analysis conducted, the project drew a conclusion and recommended the architecture that best met the design requirements. Overall, selecting the appropriate tools, language, and techniques for designing and implementing digital circuits is crucial in achieving an optimal design that meets the desired performance requirements.

##### *RTL schematics*

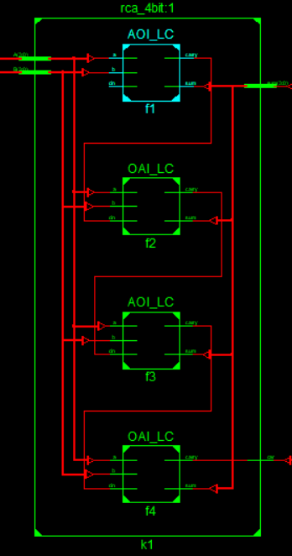
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Figure 3 RTL schematic of conventional RCA based BTA

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Figure 4 AOI\_OAI based BTA

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Figure 6 BTA using carry\_select\_adder

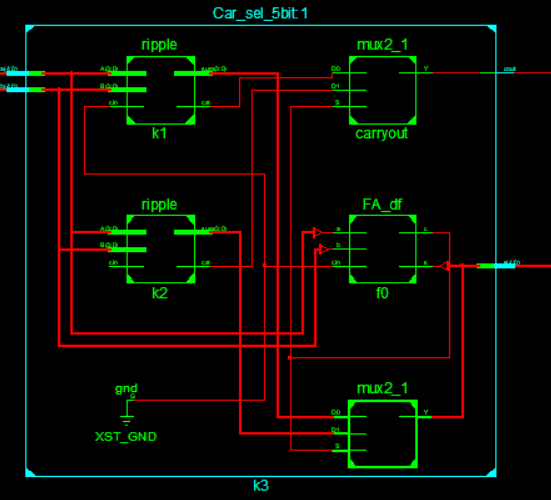


Figure 7 Carry select adder

# Simulation Results

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Figure 8 IO Luts and Slice utilization

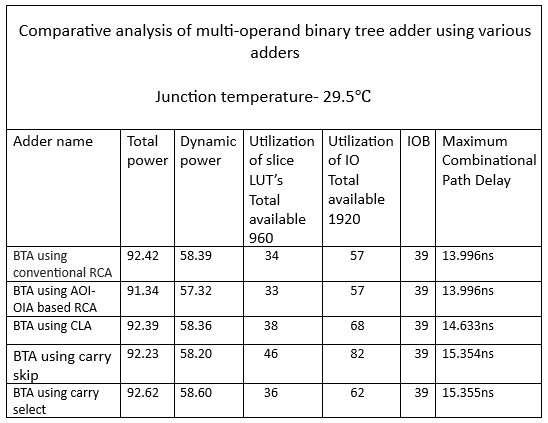
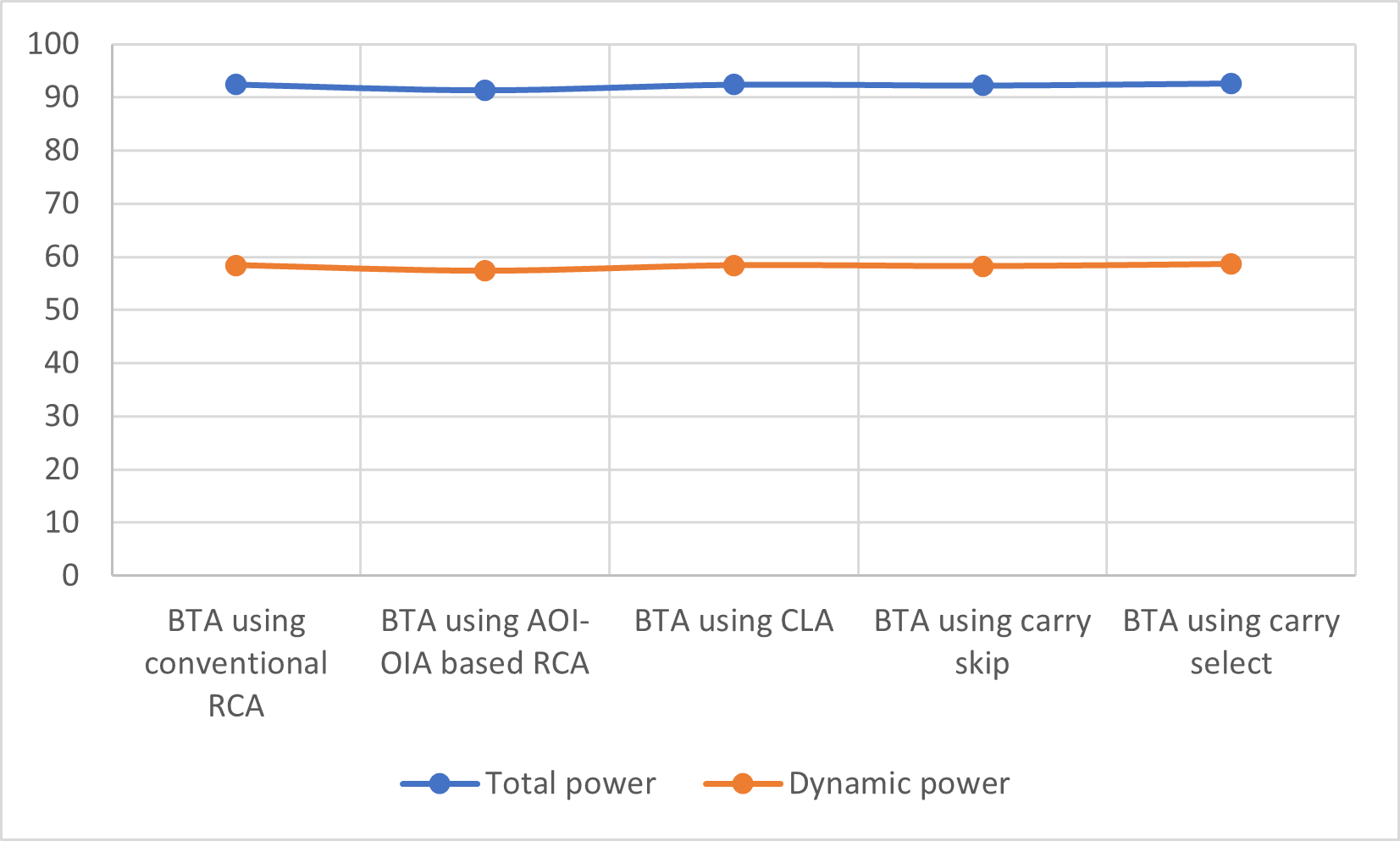
 

Figure 9 Dynamic Power and static power comparison

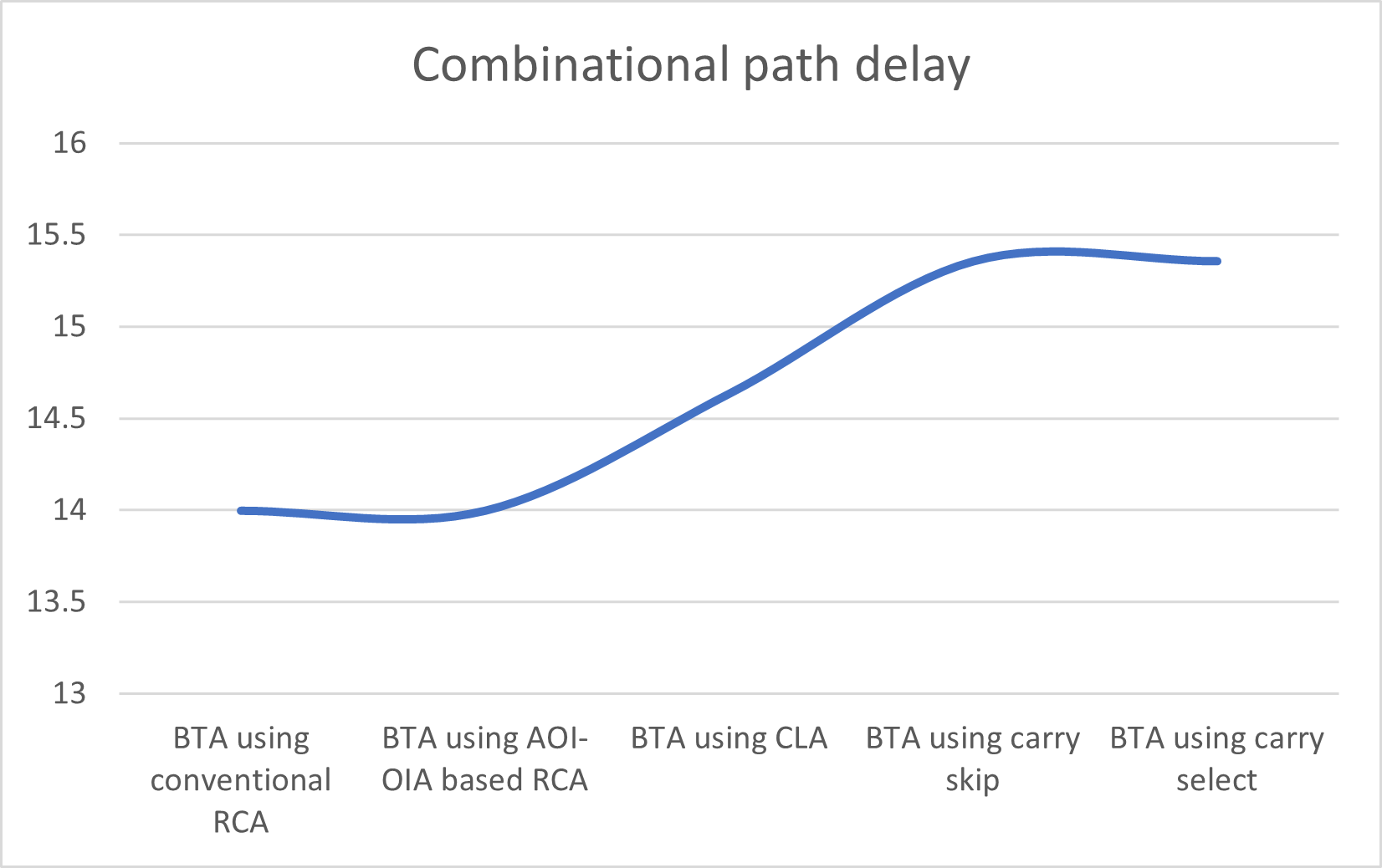


Figure 10 Comparison of combinational path delay for different architectures

# Conclusion

# References